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AUPEC 06

Reference number: 49

Dear Ali A-Ghadimi,

Your paper entitled “Detailed Modeling and analysis of a full bridge PWM DC-DC converter” has been fully peer reviewed by specialist national and/or international reviewers. On behalf of the Technical Committee, it is my pleasure to inform you that the paper has now been **accepted** for presentation at the Conference and for inclusion in the Conference Proceedings. We would like to invite you and your colleagues to participate in AUPEC 06 which is to be held in Melbourne, Australia from December 10 to 13, 2006.

Reviewer’s reports are attached with this email. Please submit your revised paper to AUPEC06 technical secretariat by 16 October 06 addressing the questions/comments raised by the reviewers. If your paper does not require any changes based on the reviewers report, we will record your submitted full paper as the final paper for the conference.

Unless one of the authors of an accepted paper registers for the conference, the paper will not be published in the conference proceedings.

If you wish to present more than one paper at the conference, please note that a **fee of $100 per additional paper** will be charged to cover the cost of inclusion in proceedings. **The page limit is six pages per paper** and any paper which exceeds this limit will be charged a page **fee of $100 per additional page**.

The details on author's presentation guidelines will be available on the AUPEC'06 website shortly. Presenting authors are required to submit a brief biography (50-100 words) by 30th October, 2006 to the conference secretariat. Registration forms are available on the AUPEC'06 website at http://www.staff.vu.edu.au/aupec2006/registration.htm .

Accommodation information is available on the AUPEC'06 website at: http://www.staff.vu.edu.au/aupec2006/accomodation.htm . Please send any enquiries regarding your paper or the conference to amanullah.maungthanoo@research.vu.edu.au.

As December period is a busy period in Melbourne, it will be advisable to book accommodation at the earliest. The latest information on the conference including the programme will be posted on the conference homepage.

Kind regards,

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Detailed Modelling and Analysis of a Full Bridge PWM DC-DC Converter

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ABSTRACT

This paper presents a detailed small-signal and transient analysis of a full bridge PWM converter designed for high voltage, high power applications using an average model. The derived model is implemented in a typical system and used to produce the small-signal and transient characteristics of the converter. Results obtained in the analysis of the high voltage and high power design example is validated by comparison for actual system with multiple switch and proposed model and show that the proposed model responses are identical to actual one and therefore the derived model can be used for performance analysis of the circuit and also design of controller.

1. INTRODUCTION

Today, new advances in power generation technologies and new environmental regulations encourage a significant increase of distributed generation resources around the world. Distributed generation systems (DGS) have mainly been used as a standby power source for critical businesses. For example, most hospitals and office buildings had stand-by diesel generators as an emergency power source for use only during outages. However, the diesel generators were not inherently cost-effective, and produce noise and exhaust that would be objectionable on anything except for an emergency basis. On the other hand, environmental-friendly distributed generation systems such as fuel cells, micro turbines, biomass, wind turbines, hydro turbines or photovoltaic arrays can be a solution to meet both the increasing demand of electric power and environmental regulations due to green house gas emission [1-3]. Advances in power electronics and energy storage devices for transient backup have accelerate penetration of the distributed generation into electric power generation plants.

Most of this generation's unit has DC output and in order to produce higher AC voltage than the DC output voltage, they must have a DC/DC boost converter and a DC/AC inverter as shown in figure 1.

DC-DC converters can be used to boost and regulate low output voltage of any DC source like some new distributed generation units to high voltage and compensate for its slow response during the transient. The main task of these converters is to maintain the output voltage at constant and predefined level.

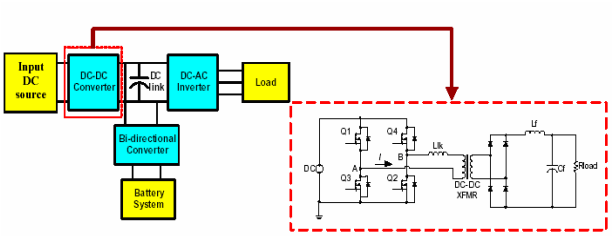

Fig. 1: Block diagram of the power conversion system

To boost low voltage DC to high voltage DC a forward boost converter, a push-pull boost converter or an isolated full-bridge DC to DC power converter can be selected. Among these power converters, Full-Bridge converters are the most attractive topology for high power generation [4-6].

For control purpose and analyzing the behavior of converter, dynamic analysis of converter must be done. The choice of the average modeling method to study both large and small-signal characteristics of modern power converters has become widely accepted due to its adaptability to computer simulation. When an average model is simulated, it requires with less computation time than the switched circuit model [5]. Dynamic performance of some PWM dc-dc converters type has been analysed using state space averaging method in continues and discrete time domain [5-8].

In this paper, a large signal and small signal model of full-bridge dc-dc converter are studied. In this study, the parasitic resistances of switches are considered.

This paper is presented in seven sections. In Section 2, a discussion of Full-Bridge converter's operation is presented and in Section 3 the average model is described. The validity of derived model is verified by mean of simulation in section 4. Steady state analysis and dynamic model are in section 5, and in section 6 the proposed average model is validated by comparison to the switched circuit model. Finally in section 7, the conclusion of paper is presented.

2. FULL-BRIDGE CONVERTER OPERATION

Figure 2 shows the circuit schematics of a full bridge converter that consist of a full bridge power converter (Q1 to Q4), a high frequency transformer (ratio 1:n), a bridge diode, and an output filter (L,C). The diagonally opposite switches (Q1 and Q2, or Q3 and Q4) are turned on and off simultaneously in a portion of each half cycle of switching frequency as shown in Figure 2 (for time interval $D.T_S$. When all four switches are turned off, the load current freewheels through the rectifier diodes (for time interval $T_S/2$-DT_S [9].

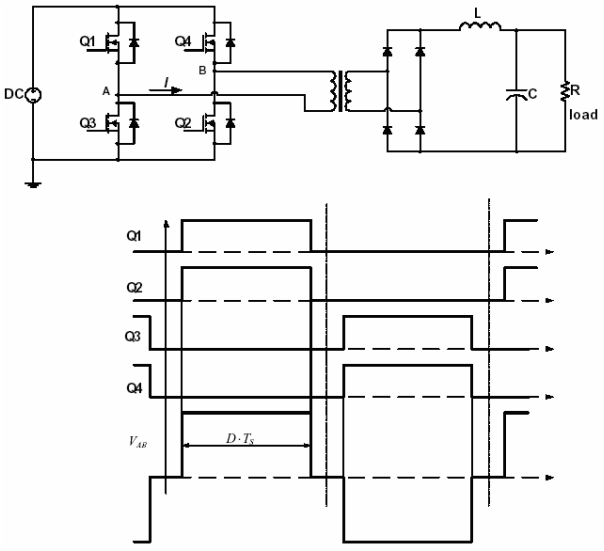

Figure 2: operation of full bridge converter

The PWM pulse generator has input of Duty Cycle (D) and will produces appropriate pulses and sends them to switches. Figure 3 shows signal waveform for producing appropriate pulses according to desired duty cycle (D).

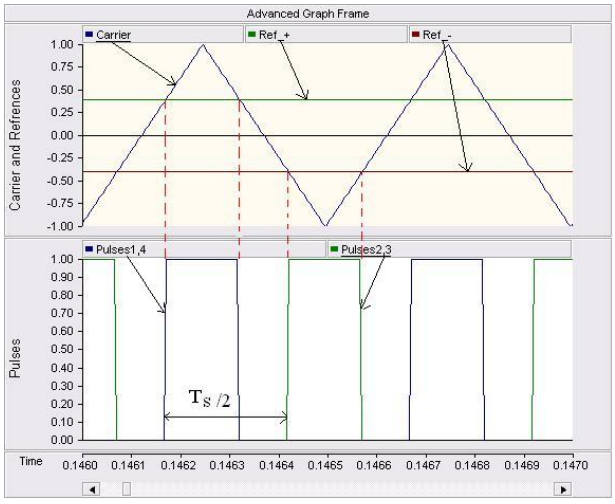

Figure 3: PWM Generation for Full Bridge Converter

As shown in figure 3, a constant signal (Reference) is compared with a rectangular high frequency signal (Carrier). When carrier signal go over reference signal a pulse will produce and similarly negative value of reference signal will compare with carrier for producing other half cycle pulse. As shown in this figure by changing reference signal from 0 to 1 we can have pulse with duty cycle of $0.5*T_S$ to zero. This two pulse give to pair of switch and the switch will conduct in each half period with duration of DT_S.

In order to reduce the size and the weight of magnetic components, it is desirable to increase the switching frequency for DC-DC converters. However, when the switching frequency is increased, switching losses would increase, and snubbers and protection are required, which introduce significant losses and lower the efficiency.

3. DERIVING AVERAGED MODEL FOR FULL-BRIDGE CONVERTER

For modeling the full bridge converter and driving averaged model, it is assumed:

1- Transistor and diodes are identical
2- Transistors and diodes have on resistance r_T, r_D respectively.
3- The output filter so designed that inductor current is continues in each switching period.
In this circuit, there is two state variable including capacitor voltage and inductor current.

As illustrated in previous section, full bridge converter has 2 mode of operation in each half cycle:

3.1. MODE 1: $T_0<T<T_{ON}$

In this mode, switches Q1 and Q2 are on and delivering energy to load via transformer and two diodes. For this mode, the circuit model is as shown in figure 4. Using KVL and KCL, we can derive the state equation of the circuit as presented below. In this model the state variable are inductance current (X_1) and capacitor voltage (X_2):

$$KVL: \quad nV_d = R_{th}X_1 + L\dot{X}_1 + X_2$$
$$KCL: \quad X_1 = C\dot{X}_2 + \frac{X_2}{R} \qquad (1)$$
$$where \quad R_{th} = 2n^2 r_T + 2r_D$$

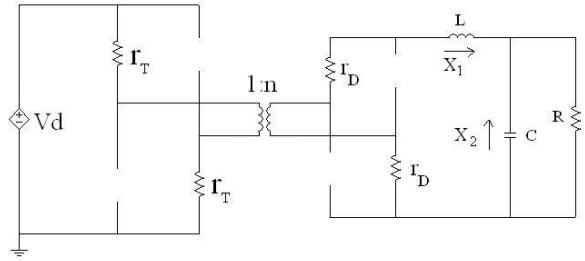

Figure 4: Mode 1 of operation

Therefore the state space model and matrices in the interval $d.T_s$ are:

$$\dot{X} = A_1 X + B_1 V_d \qquad , \qquad V_0 = C_1 X$$

$$A_1 = \begin{bmatrix} -\frac{R_{th}}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \qquad (2)$$

$$B_1 = \begin{bmatrix} \frac{n}{L} \\ 0 \end{bmatrix}$$

$$C_1 = \begin{bmatrix} 0 & 1 \end{bmatrix}$$

3.2. MODE 2: $T_{ON}<T<T_S/2$

In this mode, all switches are off and load current flow through bridge diodes and circuit can be modeled as figure 5.

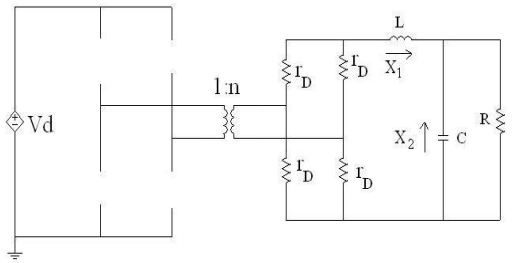

Figure 5: Mode 2 of operation

Again there are following equation:

$$KVL: \quad 0 = r_D X_1 + L\dot{X}_1 + X_2$$
$$KCL: \quad X_1 = C\dot{X}_2 + \frac{X_2}{R} \qquad (3)$$

And therefore state matrices in this mode are:

$$A_2 = \begin{bmatrix} -\frac{r_D}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \qquad B_1 = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \qquad C_1 = \begin{bmatrix} 0 & 1 \end{bmatrix} \qquad (4)$$

Finally, based on averaged model concept [5,9], and because the last half cycle is identical to first half, we can obtain averaged model of this converter in Ts/2 as:

$$\dot{X} = AX + BV_d \qquad , \qquad V_0 = CX$$

$$A = A_1 2d + A_2(1-2d) = \begin{bmatrix} -\frac{R_{th}2d + r_D(1-2d)}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \qquad (5)$$

$$B = B_1 2d + B_2(1-2d) = \begin{bmatrix} \frac{2dn}{L} \\ 0 \end{bmatrix}$$

$$C = C_1 2d + C_2(1-2d) = \begin{bmatrix} 0 & 1 \end{bmatrix}$$

This averaged model state equation can be used for simulation of converter instead of the model with multiple switches that may have long simulation time and also this state equation can used for analysis of original one performance and development of controller and stability studies.

Based on above average model, the following electrical circuit model can be derived and used for simulation, design of controller, and stability studies.

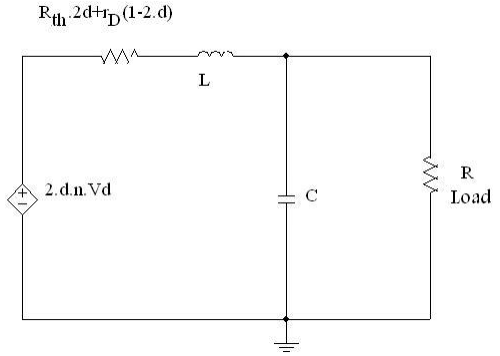

Figure 6: Large signal averaged model of Full Bridge Converter

4. MODEL VALIDATION

To validate the proposed method, we studied a 5 KW system with the parameter shown in table 1. PSCAd/EMTDC that is an industry standard simulation tool for studying the transient behavior of electrical networks [10] is used for simulation. In this study, the Output filter of the converter is so designed that there is 2% ripple in inductor current and 1% ripple in output voltage [11].

Table 1: System Parameter

Input Voltage Vd (Volts)	50	Filter Inductance L (mH)	7
Transformer Power (KVA)	5	Filter Capacitance C (micro Farad)	330
Transformer Voltages	50:500	Load Resistance (ohms)	12.5
Switching Frequency (Hz)	2000	Switches on Resistor (ohms)	5e-3

For verifying the proposed model, simulation with actual system and averaged model in large signal in 3 study cases performed:

4.1. STEP CHANGE IN DUTY CYCLE (D)

In this case the actual system and averaged model simulated with d=0.2 and then in time 1 seconds the duty cycle change from 0.2 to 0.3. Figure 7 shows the simulation results for this case and the actual model and actual result represented together for compare. Results show near perfect agreement, with the average model closely tracking those of the actual circuit and the model is valid in this large signal change in duty cycle (D).

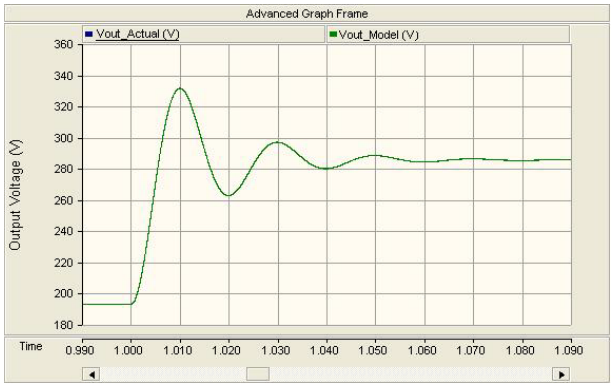

Figure 7: Step change in duty cycle from 0.2 to 0.3 and output voltage in modelled system and actual one

4.2. CHANGE IN LOAD

In this case a load transient from 100% to 50% full load is simulated at 1 second by turning off the load switch. Results from the transient simulation from both methods are shown superimposed in figure 8. As the figure shows, two waveforms are exactly identical and it is impossible to separate them. The figure also shows that output voltage drop when load is increased in this open loop system.

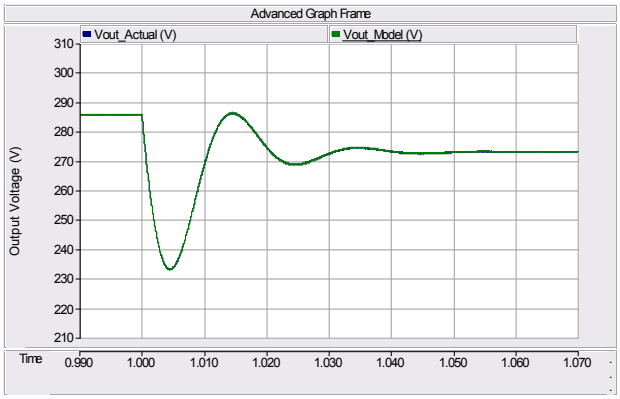

Figure 8: Simulation results for step change in load

4.3. CHANGE IN INPUT VOLTAGE

In final case study, a change in input voltage from 50 volts to 40 volts in time 0.5 sec. is simulated and the results show two waveforms are identical that means the output voltage is both model are identical.

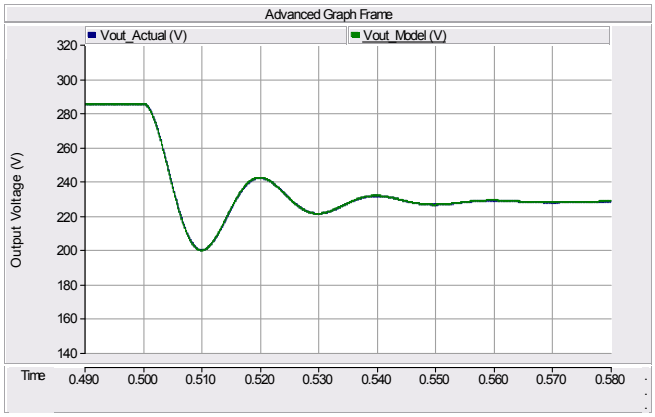

Figure 9: Simulation waveform for step change in input voltage

5. STEADY-STATE ANALYSIS

With the model of state space equation and matrices A,B,C we can consider small ac perturbation (represented by ~) and dc steady state (In upper case letters) quantities for model parameter as:

$$\begin{aligned} x &= X + \tilde{x} \\ v_o &= V_o + \tilde{v}_o \\ d &= D + \tilde{d} \\ v_d &= V_d + \tilde{v}_d \end{aligned} \tag{6}$$

Substitution of this parameter into state equation (Eq. 5) yield:

$$\begin{aligned} &\dot{\tilde{x}} = AX + BV_d + (A\tilde{x} + B\tilde{v}_d) + [(A_1 - A_2)X + (B_1 - B_2)V_d]2\tilde{d} \\ &+ terms\ with\ product\ of\ \tilde{x}, \tilde{d}, \tilde{v}_d (negligible) \\ &V_o + \tilde{v}_o = CX + C\tilde{x} + [(C_1 - C_2)X]2\tilde{d} \\ &+ terms\ with\ product\ of\ \tilde{d}, \tilde{v}_d (negligible) \end{aligned} \tag{7}$$

The steady state equation can be obtained from Eq. 7 by setting all ac components to zero. Therefore the steady state equation is:

$$\begin{aligned} &AX + BV_d = 0 \\ &and\ \ for\ output: V_o = CX \end{aligned} \tag{8}$$

And therefore in Eq. 7 the small signal components have this relation:

$$\begin{aligned} &\dot{\tilde{x}} = A\tilde{x} + B\tilde{v}_d + [(A_1 - A_2)X + (B_1 - B_2)V_d]2\tilde{d} \\ &\tilde{v}_o = C\tilde{x} + [(C_1 - C_2)X]2\tilde{d} \end{aligned} \tag{9}$$

Using Eq. 8 and value of matrices in Eq. 5 the steady state dc voltage transfer function is:

$$m = \frac{V_o}{V_d} = -CA^{-1}B = 2Dn\frac{R}{R + R_{th}2D + r_D(1-2D)} \tag{10}$$

Figure 10 show the dc output to input gain (m) versus duty cycle (D) in several load resistance. As the figure shows there is approximately linear relationship between dc gain and duty cycle and as we increase D from 0 to 0.5 output voltage to input voltage gain will increase approximately in a linear manner.

From the curves, it is clear that an increase in load (by decreasing load resistance) result in a decreased gain for a constant duty cycle. Therefore, the steady state voltage must be regulated by changing duty cycle (D).

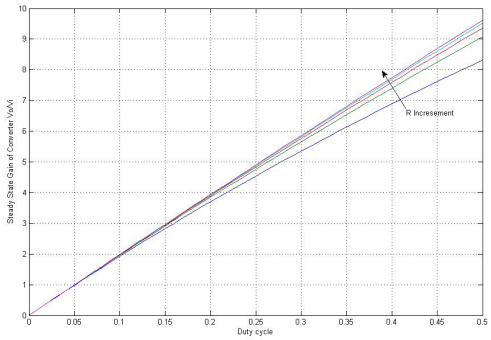

Figure 10: Steady state gain of converter in various Load resistance versus D

6. SMALL SIGNAL ANALYSIS

From Eq. 9 that consists of ac perturbations and using laplace transform:

$$\tilde{x}(s) = (SI - A)^{-1}[(A_1 - A_2)X + (B_1 - B_2)V_d]2\tilde{d}(s) + (SI - A)^{-1}B\tilde{v}_d(s) \qquad (11)$$
$$\tilde{v}_o(s) = C\tilde{x}(s) + [(C_1 - C_2)X]2\tilde{d}(s)$$

From Eq. 11 we can obtain output voltage laplace transform in term of input voltage and duty cycle:

$$\tilde{v}_o(s) = \{C(SI - A)^{-1}[(A_1 - A_2)X + (B_1 - B_2)V_d] + (C_1 - C_2)X\}2\tilde{d}(s) + C(SI - A)^{-1}B \quad \tilde{v}_d(s) \qquad (12)$$

For obtaining transfer function of output voltage to duty cycle, the perturbation of input voltage is assumed to be zero and therefore:

$$\frac{\tilde{v}_o(s)}{\tilde{d}(s)} = 2C(SI - A)^{-1}[(A_1 - A_2)X + (B_1 - B_2)V_d] + 2(C_1 - C_2)X \qquad (13)$$

Substituting matrices from Eq. 5 and simplification, the transfer function of Eq. 13 can be derived as Eq. 14:

$$\frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{2}{LC}\ \frac{nV_d + (r_D - R_{th})X_1}{den(s)}$$

Where:

$$\text{den(s)} = s^2 + (\frac{1}{RC} + \frac{R'}{L})s + (\frac{R'}{RLC} + \frac{1}{LC}) \qquad (14)$$

$$and \quad R' = R_{th}2D + r_D(1 - 2D)$$

V_d, X1, D are steady state value for input voltage, inductance current and duty cycle respectively.

Based on the small signal model derived in previous section, it can be seen that the full bridge converter acts like a second order system. But as transfer function equation shows, dynamic of converter depend on operating point, since in the model inductor current and duty cycle steady state value of operating point exist.

To validate the average model a step change in duty cycle (d from 0.3 to 0.28) has been introduced and the results are shown in figure 11.

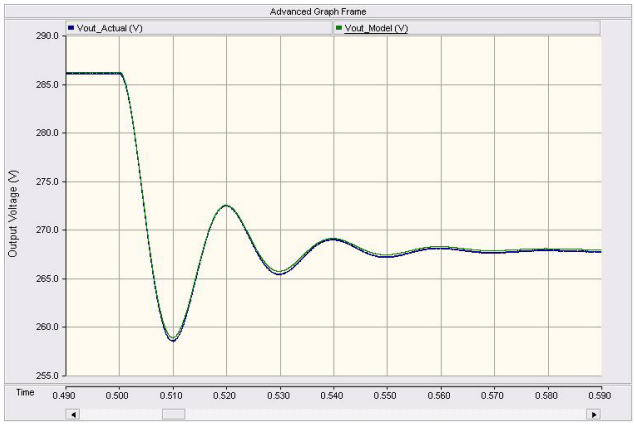

Figure 11: Small signal model and actual model simulation for change 0.02 in d

Asshown in figure 11, the derived small signal response is very close to the switched circuit model; hence the transfer function can be used for dynamic analysis of the converter and designing controller.

Another case is studied for a large change in duty cycle from 0.3 to 0.2, and result of voltage for this case is shown in figure 12. As figure show in this case the small signal model has a small difference with actual one but this difference is very small.

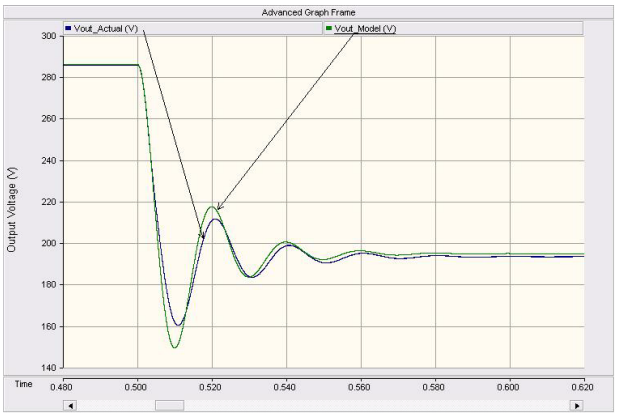

Figure 12: Small signal model and actual model simulation for change 0.1 in d

According to small-signal characteristics of this converter, compensation techniques for output voltage control are needed.

7. CONCLUSION

This paper presents an averaged model for full bridge dc-dc converter. The model used for steady state, dynamic analysis, and large signal analysis of this converter. The developed models are used to study the characteristics and dynamics of full bridge converter. The approach is applicable to simulation and controller design. Simulation results for the full bridge converter show the feasibility of the proposed model for steady-state analysis and small signal analysis and verify the derived model. Validation of the derived model is based on a comparison of dc, small-signal, and large-signal simulation results to those obtained from the simulation of the actual circuit.

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